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<p>(21) International Application Number: PCT/AU99/00979</p> <p>(22) International Filing Date: 8 November 1999 (08.11.99)</p> <p>(30) Priority Data: PP 6997 6 November 1998 (06.11.98) AU</p> <p>(71) Applicant (for all designated States except US): PACIFIC SOLAR PTY LIMITED [AU/AU]; 82-86 Bay Street, Botany, NSW 2019 (AU).</p> <p>(72) Inventors; and (75) Inventors/Applicants (for US only): SHI, Zhengrong [AU/AU]; 37 Princes Mary Street, Beacon Hill, NSW 2100 (AU). GREEN, Martin, Andrew [AU/AU]; 10 Blandford Avenue, Waverley, NSW 2024 (AU). WENHAM, Stuart, Ross [AU/AU]; 13 Von Nida Place, Menai Heights, NSW 2234 (AU). BASORE, Paul, Alan [AU/AU]; 127 Taren Road, Caringbah, NSW 2229 (AU). JI, Jing, Jia [AU/AU]; 2/130-132 Croydon Road, Croydon, NSW 2132 (AU).</p> <p>(74) Agent: F B RICE & CO; 605 Darling Street, Balmain, NSW 2041 (AU).</p>		<p>(81) Designated States: AE, AL, AM, AT, AU, AZ, BA, BB, BG, BR, BY, CA, CH, CN, CR, CU, CZ, DE, DK, DM, EE, ES, FI, GB, GD, GE, GH, GM, HR, HU, ID, IL, IN, IS, JP, KE, KG, KP, KR, KZ, LC, LK, LR, LS, LT, LU, LV, MA, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SL, TJ, TM, TR, TT, TZ, UA, UG, US, UZ, VN, YU, ZA, ZW, ARIPO patent (GH, GM, KE, LS, MW, SD, SL, SZ, TZ, UG, ZW), Eurasian patent (AM, AZ, BY, KG, KZ, MD, RU, TJ, TM), European patent (AT, BE, CH, CY, DE, DK, ES, FI, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, GW, ML, MR, NE, SN, TD, TG).</p> <p>Published With international search report.</p>
<p>(54) Title: THIN FILMS WITH LIGHT TRAPPING</p> <div data-bbox="342 1157 1263 1709"> </div> <p>(57) Abstract</p> <p>A thin film silicon solar cell is provided on a glass substrate (11), the glass having a textured surface (12), including larger scale surface features (13) and smaller scale surface features (14). Over the surface (12) is deposited a thin barrier layer (31) which also serves as an anti-reflection coating. The barrier layer may be a silicon nitride layer for example and will be 70 nm± 20 % in order to best achieve its anti-reflection function. Over the barrier layer (31) is formed an essentially conformal silicon film (15) having a thickness which is less than the dimensions of the larger scale features of the glass surface and of a similar dimension to the smaller scale features of the glass surface.</p>		

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*Thin Films with light trapping***Introduction**

The present invention relates generally to thin film photovoltaic devices and in particular the invention provides a structure and a method of forming the structure for thin film cells to achieve light trapping in these cells.

Background of the Invention

The use of light trapping is well known in monocrystalline silicon cells where light trapping features in the surface of the cell have dimensions which are much less than the thickness of silicon substrate of the device and significantly greater than the wavelength of light in air.

10 In solar cells, light scattering is used to trap light in the active region of the cell. The more light that is trapped in the cell, the higher the efficiency that can be obtained. Therefore, light trapping is an important issue when trying to improve efficiency in solar cells and is particularly important in thin film cell design.

15 However it has been widely thought that in thin film devices where the active silicon layers are thin films formed over a substrate such as glass, light trapping would not be possible or at least demonstrate reduced effectiveness. This is because the film thicknesses are of the same order of magnitude or thinner than the dimension of light trapping features in known
20 monocrystalline devices. As film thicknesses in thin film devices are reduced, they tend toward conformal coatings having predominantly parallel surfaces over the etched surface of the glass substrate and conventional thinking would be that such an arrangement does not achieve significant advantages from light trapping. Also as film thicknesses are reduced to the order of a wavelength (in
25 air) or thinner conventional thinking is that the mechanisms providing light trapping in prior art devices would cease to be effective.

This is borne out in prior art thin film amorphous silicon solar cell devices where no deliberate attempt at texturing was made. Present day amorphous silicon devices typically comprise a glass superstrate over which is
30 layed a Transparent Conductive Oxide (TCO) contact layer and a thin amorphous silicon film (1 μ m) active layer including a p-n junction and a rear metallic layer acting as a reflector and back contact. When such structures were first devised it was noticed that in some circumstances (when the surface of the TCO was cloudy) cell performance was greater than expected but the

literature offered no explanation as to the reason for such unexpected performance.

It has now become apparent to the present inventors that light trapping is possible in thin film devices and the prior art amorphous silicon devices were in fact demonstrating a characteristic that the present inventors have now identified and adapted to crystalline silicon thin film cells. Central to the invention is the realisation that the wavelength of light of a given frequency is different in silicon and air.

The present inventors have now identified the circumstances under which light trapping can be achieved in thin films and in particular the inventors have devised methods for manufacture of thin film crystalline silicon solar cell structures which exhibit light trapping characteristics.

Summary of the Invention

According to a first aspect, the present invention provides a method of forming a light trapping structure in a thin film silicon solar cell formed on a glass substrate or superstrate, the method including the steps of:

- a) etching a surface of the glass substrate or superstrate to provide a textured surface; and
- b) forming a silicon film on the textured surface and forming a photovoltaic device structure in the silicon film, the silicon film being less than 10µm thick.

According to a second aspect, the present invention provides a thin film photovoltaic device incorporating a light trapping structure, wherein the photovoltaic device is formed on a textured surface of a glass substrate or superstrate, the photovoltaic device comprising a thin silicon film into which is formed at least one pn photovoltaic junction, the silicon film being less than 10µm thick.

The invention is applicable to both crystalline and amorphous silicon solar cells. In the case of amorphous silicon devices, a Transparent Conducting Oxide (TCO) layer will be formed immediately below the silicon film.

In embodiments of the invention, the textured surface of the glass preferably includes surface features having dimensions in the range of from 0.05-0.2 times the thickness of the silicon film. Preferably also, a thin conformal barrier layer is formed between the textured glass surface and the silicon film to prevent migration of contaminants from the glass to the silicon.

The barrier layer may also act as an anti-reflection layer and will in that case, be arranged to have a thickness equal to a quarter wavelength $\pm 20\%$ which in the case of silicon nitride is $70 \text{ nm} \pm 20\%$

5 The silicon film is typically less than $5\mu\text{m}$ thick and preferably has a thickness of $2\mu\text{m}$ or less. The silicon film is typically at least $0.5\mu\text{m}$ or greater and preferably greater than $1\mu\text{m}$. Typically, the scale of textured surface features is in the range of $0.01\text{-}10\mu\text{m}$. The useful lower limit of the feature size is in the order of a wavelength of light in crystalline silicon and typically the useful lower limit is $0.05\mu\text{m}$. The texturing may also include large scale
10 features which have dimensions greater than the thickness of the silicon film.

In some embodiments of the invention, the surface of the substrate is textured by an etching step, which is performed to form features in the substrate surface having a range of dimensions including dimensions which are greater than the thickness of the silicon film structure. In preferred
15 embodiments these features are in the range of $1\text{-}5\mu\text{m}$ on average and typically in the order of $2\mu\text{m}$.

Where such an etching step is employed it is performed in a manner to additionally provide small scale surface features which have dimensions significantly less than the thickness of the silicon film structure. Typically,
20 the small scale surface features will vary in the range of $0.01\text{-}1\mu\text{m}$.

In one embodiment of the invention, the etching step is performed by applying an etching composition which includes HF or a derivative thereof to the glass surface to be etched.

The glass substrate, after etching using HF may be optionally
25 subsequently heated to a temperature at which the glass softens and angular edges of the surface features are rounded. An application of a layer of spin-on glass, can also be used instead of thermal rounding of the etched glass surface.

In typical embodiments of the invention the back surface of the silicon film structure (ie, remote from the glass) has a reflective material formed over
30 it. Typically, the reflective material will be a metallisation structure used to contact the active regions of the cell. The metallisation structure will in some embodiments, be separated from most of the silicon back surface by an insulating layer.

Brief Descriptions of the Drawings

Embodiments of the invention will now be described by way of example, with reference to the accompanying drawings in which:

Figure 1 is a sectional side view of a glass surface etched in accordance with a first embodiment, with a silicon layer formed over the etched surface;

Figure 2 is a sectional side view of a glass surface etched in accordance with a second embodiment, with a silicon layer formed over the etched surface;

Figure 3 is a sectional side view of a glass surface similar to that of Figure 1, but to which a step of heating the glass to its softening point has been performed after the etching step and before the silicon layer was applied;

Figure 4 is a sectional side view of a glass surface similar to that of Figure 2, but to which a step of heating the glass to its softening point has been performed after the etching step and before the silicon layer was applied;

Figure 5 is a sectional side view of a glass substrate with a textured surface layer and a thin film of silicon formed over its surface, illustrating representative paths of incident photons through the glass substrate, and the silicon layer;

Figures 6 and 7 are photographs of sections through a thin silicon film formed over an etched glass surface in accordance with an embodiment of the invention; and

Figures 8 and 9 are sectional side views of embodiments similar to those of Figures 3 & 4, but in which a spin-on-glass layer has been employed instead of using thermal rounding.

Detailed Description of Embodiments of the Invention

Referring to Figure 1, a detailed sectional side view of a small section of a glass sheet 11 is illustrated, the glass having a textured surface 12, including larger scale surface features 13 and smaller scale surface features 14. Over the surface 12 is deposited a thin barrier layer 31 which also serves as an anti-reflection coating. The barrier layer may be a silicon nitride layer for example and will be $70 \text{ nm} \pm 20\%$ in order to best achieve its anti-reflection function. Over the barrier layer 31 is formed an essentially conformal silicon film 15 having a thickness which is less than the dimensions of the larger scale features of the glass surface and of a similar dimension to the smaller scale features of the glass surface. Typically, the larger dimension features 13 will have dimensions in the range of $1\text{-}10\mu\text{m}$, the smaller dimension features 14

will have dimensions in the range of 0.01-1 μ m and the silicon film 15 will have a thickness in the range of 0.5-5 μ m.

To achieve the structure of Figure 1, the surface of the glass sheets is first cleaned and then etched with an etching composition containing HF or a derivative thereof. The etching composition also contains an additive such as Barium Sulphate (BaSO_4) which forms deposits on the surface of the glass 11 to be etched. The etching composition covers the surface of the glass to a significant depth (say 0.1-0.5mm). During the etching process, deposits of Barium Sulphate crystals form on the surface of the glass 11, and mask the surface of the glass 11, such that the surface is selectively etched by the HF to form the larger scale features 13 and the smaller scale features 14 of Figure 1.

Typical examples of formations of the etching composition are as follows:-

Example 1 (for soft glasses)

A paste is made by mixing

Barium Sulphate (BaSO_4)	50g
Ammonium BiFluoride (NH_4) HF_2	100g
Water (H_2O)	120ml

Example 2 (for soft glasses)

A paste is made by mixing

Barium Sulphate (BaSO_4)	75g
Ammonium BiFluoride (NH_4) HF_2	75g
Water (H_2O)	100ml

Example 3 (for hard glasses)

A paste is made by mixing

Barium Sulphate (BaSO_4)	50g
Hydrofluoric Acid 50% Solution ($\text{HF}:\text{H}_2\text{O}$)	50ml

In one embodiment of the invention, after the glass has been etched, and the etchant cleaned off by washing, the silicon film 15 is formed on the surface prior to making a photovoltaic device.

In an alternative embodiment, an additional step is performed after etching and prior to formation of the silicon film, in which the glass substrate is softened by heating to a point where sharp surface features are rounded as

illustrated in Figure 3. The sharper features of the surface texture can in some instances hinder the later processing of the photovoltaic cell structure created in the thin silicon film formed on the glass substrate. The rounding of these features reduces the difficulties created by the sharper surface features where shunting often occurs in thin film junctions formed on the textured surface due to the excessive thinning of the active layers over sharp peaks in the texturing. By heat treating the glass, the sharpness of the peaks is reduced with a resultant significant reduction in the occurrence of shunting in the completed device.

In the case of soft glasses, the heat treatment to round the surface features involves heating the glass, or at least the surface of the glass, to a temperature of 700°C for a period of less than one hour and typically, for periods in the order of 15 minutes.

Referring to Figure 2, a detailed sectional side view of an alternative embodiment of the invention is illustrated in which a glass sheet 11 has a textured surface over which is formed a barrier layer 31 and a thin film of silicon 15. In this embodiment, the largest dimension of the surface texturing 24 is smaller than, or of the same order of magnitude as the thickness of the silicon film. Typically, in this embodiment, the largest dimension of the surface texturing is in the range of 0.1-1µm, while the thin silicon film has a thickness in the range of 0.5-2µm.

The surface texturing of the embodiment of Figure 2, is achieved in a similar manner to that of the process used to achieve the Figure 1 embodiment with smaller features being achieved by varying etch parameters such as etching solution composition, etching time/temperature and etching solution film thickness (ie, time to exhaustion).

Liquid formulations of the etching composition are achieved by adding water (H₂O) and/or hydrofluoric acid to any of the examples mentioned previously until the required strength and consistency is achieved.

As with the previous embodiment, the etching composition is washed from the surface of the glass before the thin silicon film is formed over the textured surface. Referring to Figure 4, a further alternative embodiment is illustrated in which the glass substrate has been softened by heating after etching as with the embodiments of Figure 3, such that sharper surface features are rounded.

Finally, as illustrated in Figure 5, which is a sectional view of an embodiment similar to those of Figures 1-4, after the silicon has been formed and any processing required to be performed over the entire silicon layer has been completed, such as the formation of a dielectric layer 19, a metal layer 40 is applied over the silicon surface 36 to provide a back reflector and to be processed into contacts for contacting to the semiconductor device formed in the silicon film. The dielectric layer 19 is located between the silicon 15 and the metal layer 40 in order to isolate the metal from the upper region (p-type in this example) of the semiconductor film such that portions of the metal can be connected through to the lower region (n-type in this case) of the semiconductor film without shorting the p-n junction.

Figure 5 also illustrates some possible paths of photons of light which enter or exit the silicon film 15. The photons travel along paths 18 through the substrate and are reflected within the silicon film 15, between the glass / silicon interface 20 (or anti-reflection layer/silicon interface) and the upper silicon / dielectric interface 21 or the metal (back contact) 19. By causing several reflections to occur, the photocurrent, and therefore the conversion efficiency, of a photovoltaic cell formed in the thin silicon film is increased.

Referring to Figures 6 and 7, photographs of sections through actual thin film deposits 15 on textured surface glass 12 illustrate that while the silicon film 15 approximates a conformal coating, the surface texturing includes features which are less than the thickness of the silicon film 15 with the result that the two surfaces 20, 21 are not parallel. Because the surfaces are not parallel photons of light entering the thin silicon film 15 from the glass 11 at an angle to the surface 20 of the film will generally strike the opposite surface 21 at a point at which its angle of incidence is different to that at which it leaves surface 20. Assuming that the photon is reflected from surface 21 its angle of incidence when next meeting surface 20 will be different again with a high probability of total internal reflection occurring, such that the photon will, if it is not absorbed first, have a high probability of travelling through the thin film more than twice before escaping.

Alternative embodiments of the invention are illustrated in Figures 8 & 9 which are similar to the embodiments of Figures 3 & 4 except that instead of thermally rounding the surface of the glass 11 before applying the silicon 15, a spin-on glass layer 30 is applied in each case, whereby the valleys in the texturing are partially filled and the sharper features are rounded. The spin-on

glass layer 30 also acts as a barrier layer, although in some instances a further anti-reflection layer (not shown) may also be used.

5 It will be appreciated by persons skilled in the art that numerous variations and/or modifications may be made to the invention as shown in the specific embodiments without departing from the spirit or scope of the invention as broadly described. The present embodiments are, therefore, to be considered in all respects as illustrative and not restrictive.

CLAIMS

1. A method of forming a light trapping structure in a thin film silicon solar cell formed on a glass substrate or superstrate, the method including the steps of:
 - 5 a) etching a surface of the glass substrate or superstrate to provide a textured surface; and
 - b) forming a silicon film on the textured surface and forming a photovoltaic device structure in the silicon film, the silicon film being less than 10 μ m thick.
- 10 2. The method as claimed in claim 1, wherein the thin film silicon device is formed in a crystalline silicon thin film.
3. The method as claimed in claim 1, wherein the thin film silicon device is formed in an amorphous silicon thin film which is formed on a TCO layer.
4. The method as claimed in any one of claims 1, 2 or 3, wherein the
15 etching step is performed to produce surface texturing including features having dimensions in the range of from 0.05-0.2 times the thickness of the silicon film.
5. The method as claimed in claim 4, wherein the etching step is performed to produce surface features having dimensions falling in the range
20 of 0.01-5 μ m.
6. The method as claimed in claim 4, wherein the etching step is performed to produce surface features having dimensions falling in the range of 0.05-2 μ m.
7. The method as claimed in claim 4, wherein the etching step is
25 performed to produce small scale surface features having dimensions falling in the range of 0.1-1 μ m.
8. The method as claimed in any one of claims 4 to 7, wherein the etching step is performed to produce large scale features which have dimensions greater than the thickness of the silicon film and upon which the small scale
30 features are superimposed.
9. The method as claimed in claim 8, wherein the large scale features have dimensions in the range of 1-10 μ m.
10. The method as claimed in claim 8, wherein the large scale features have dimensions in the range of 2-5 μ m.
- 35 11. The method as claimed in any one of claims 4 to 10, wherein a thermal treatment is applied after the etching step and before the silicon film is

formed, the thermal step comprising heating the substrate or superstrate to round off angular edges of the surface features.

12. The method as claimed in any one of claims 4 to 11, wherein after the etching step, a thin conformal barrier layer is formed prior to forming the thin silicon film.

13. The method as claimed in any one of claims 4 to 10, wherein after the etching step is completed, a thin spin-on glass layer is applied over the surface features, and heated to form a dielectric coating, to round off angular edges of the surface features.

14. The method as claimed in claim 13, wherein after the step of applying a thin spin-on glass layer, a thin conformal barrier layer is formed prior to forming the thin silicon film.

15. The method as claimed in claim 12 or 14, wherein the barrier layer is applied with a thickness equal to one quarter wavelength of light in the barrier layer material $\pm 20\%$.

16. The method as claimed in claim 15, wherein the barrier layer material is silicon nitride with a thickness of 70 nm $\pm 20\%$.

17. The method as claimed in any one of claims 4 to 16, wherein the etching step is performed by applying an etching composition to the surface of the substrate or superstrate, the etching composition comprising HF or a derivative of HF.

18. The method as claimed in any one of claims 4 to 17, wherein the thin silicon film formed over the textured surface has a thickness in the range of 2-20 times the average height of the features of the surface texturing.

19. The method as claimed in any one of claims 4 to 17, wherein the thin silicon film formed over the textured surface has a thickness in the range of 5-10 times the average height of the features of the surface texturing.

20. The method as claimed in claim 7, wherein the thin silicon film formed over the textured surface has a thickness in the range of 1-2 μ m.

21. The method as claimed in any one of claims 1 to 20, wherein after the silicon film is formed, a reflective material layer is formed over a surface of the silicon film remote from the substrate or superstrate.

22. The method as claimed in claim 21, wherein an insulating layer is formed over the surface of the silicon film remote from the substrate or superstrate prior to formation of the reflective material layer.

23. The method as claimed in claim 21 or 22, wherein the reflective material layer also forms a metallisation structure to contact the active regions of the cell.
24. A thin film photovoltaic device incorporating a light trapping structure, wherein the photovoltaic device is formed on a textured surface of a glass substrate or superstrate, the photovoltaic device comprising a thin silicon film into which is formed at least one *p-n* photovoltaic junction, the silicon film being less than 10 μ m thick.
25. The device as claimed in claim 24, wherein the thin silicon film is a crystalline silicon thin film.
26. The device as claimed in claim 24, wherein the thin silicon film is an amorphous silicon thin film formed over a TCO layer.
27. The device as claimed in any one of claims 24, 25 or 26, wherein the textured surface of the substrate or superstrate includes features having dimensions in the range of from 0.05-0.2 times the thickness of the silicon film.
28. The device as claimed in claim 27, wherein the textured surface has small scale surface features having dimensions falling in the range of 0.01-5 μ m.
29. The device as claimed in claim 27, wherein the textured surface has small scale surface features having dimensions falling in the range of 0.05-2 μ m.
30. The device as claimed in claim 27, wherein the textured surface has small scale surface features having dimensions falling in the range of 0.1-1 μ m.
31. The device as claimed in any one of claims 27 to 30, wherein the textured surface has large scale features which have dimensions greater than the thickness of the silicon film and upon which the small scale features are superimposed.
32. The device as claimed in claim 31, wherein the large scale features have dimensions in the range of 1-10 μ m.
33. The device as claimed in claim 31, wherein the large scale features have dimensions in the range of 2-5 μ m.
34. The device as claimed in any one of claims 27 to 33, wherein the surface features of the textured surface have been rounded by heating the substrate or superstrate to its melting point.

35. The device as claimed in any one of claims 27 to 34, wherein, a thin conformal barrier layer is located between the textured surface step and the thin silicon film.

36. The device as claimed in any one of claims 27 to 34, wherein a thin dielectric layer, derived from Sol-Gel glass, is located between the textured surface and the thin silicon film, to round off angular edges of the surface features.

37. The device as claimed in claim 36, wherein a thin conformal barrier layer is located between the dielectric layer and the thin silicon film.

38. The device as claimed in claim 34 or 37, wherein the barrier layer has a thickness equal to one quarter wavelength of light in the barrier layer material $\pm 20\%$.

39. The device as claimed in claim 38, wherein the barrier layer material is silicon nitride with a thickness of $70 \text{ nm} \pm 20\%$.

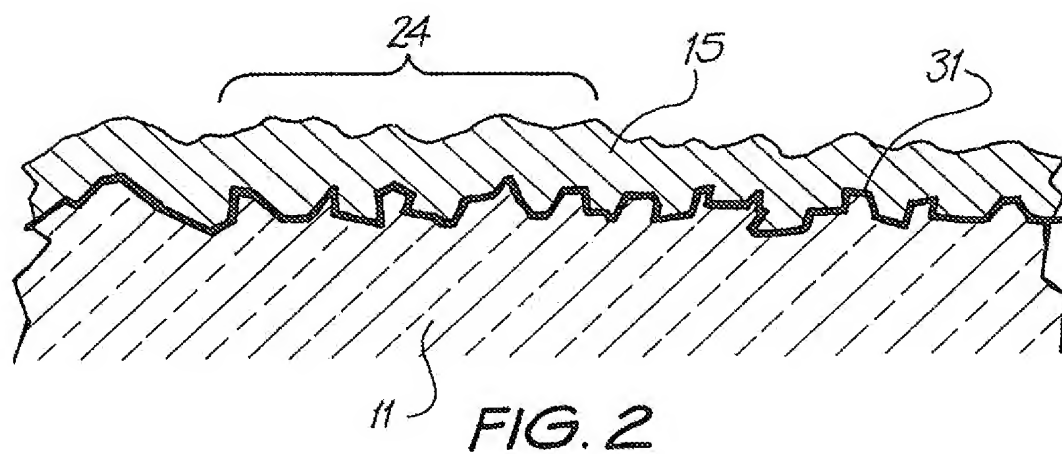
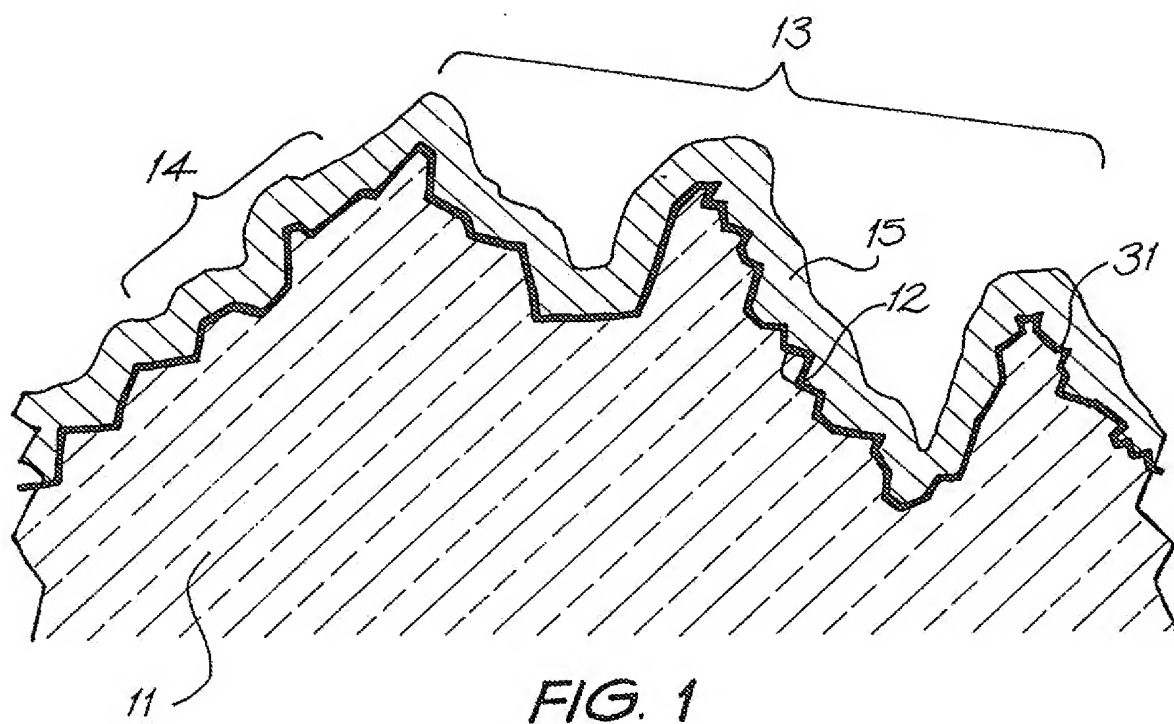
40. The device as claimed in any one of claims 27 to 39, wherein the thin silicon film formed over the textured surface has a thickness in the range of 2-20 times the average height of the features of the surface texturing.

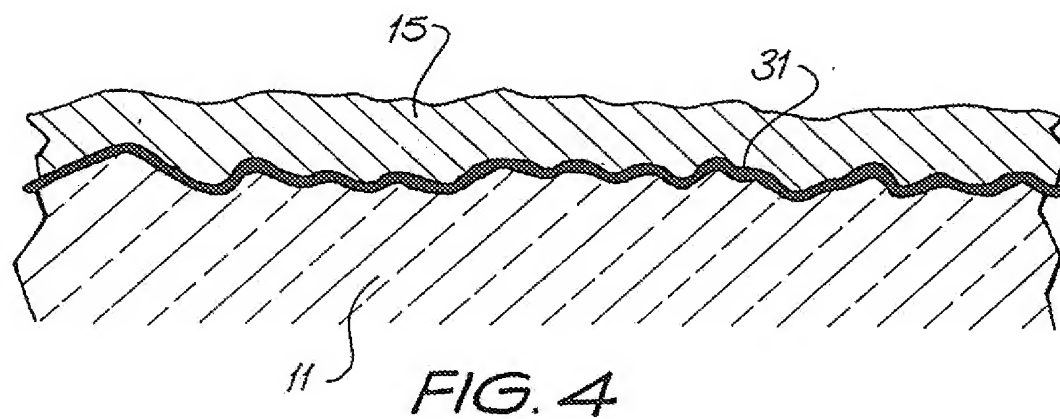
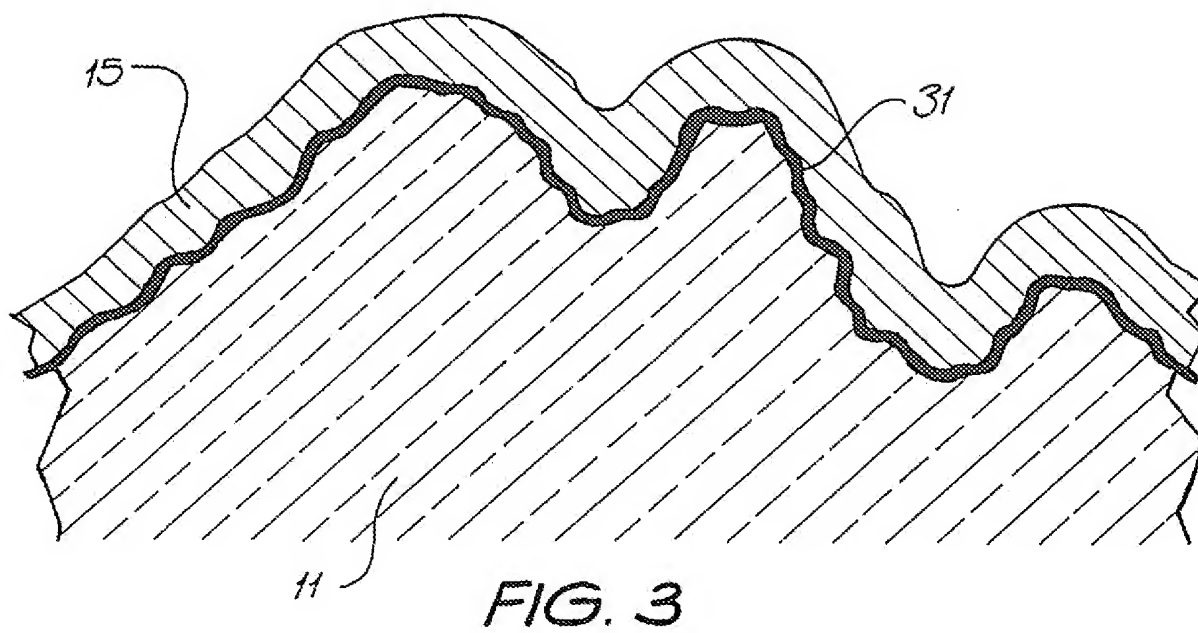
41. The device as claimed in any one of claims 27 to 39, wherein the thin silicon film formed over the textured surface has a thickness in the range of 5-10 times the average height of the features of the surface texturing.

42. The device as claimed in any one of claims 24 to 41, wherein a reflective material layer is located over a surface of the silicon film remote from the substrate or superstrate.

43. The device as claimed in claim 42, wherein an insulating layer is located between the silicon film and the reflective material layer.

44. The device as claimed in claim 41 to 43, wherein the reflective material layer also forms a metallisation structure to contact the active regions of the cell.





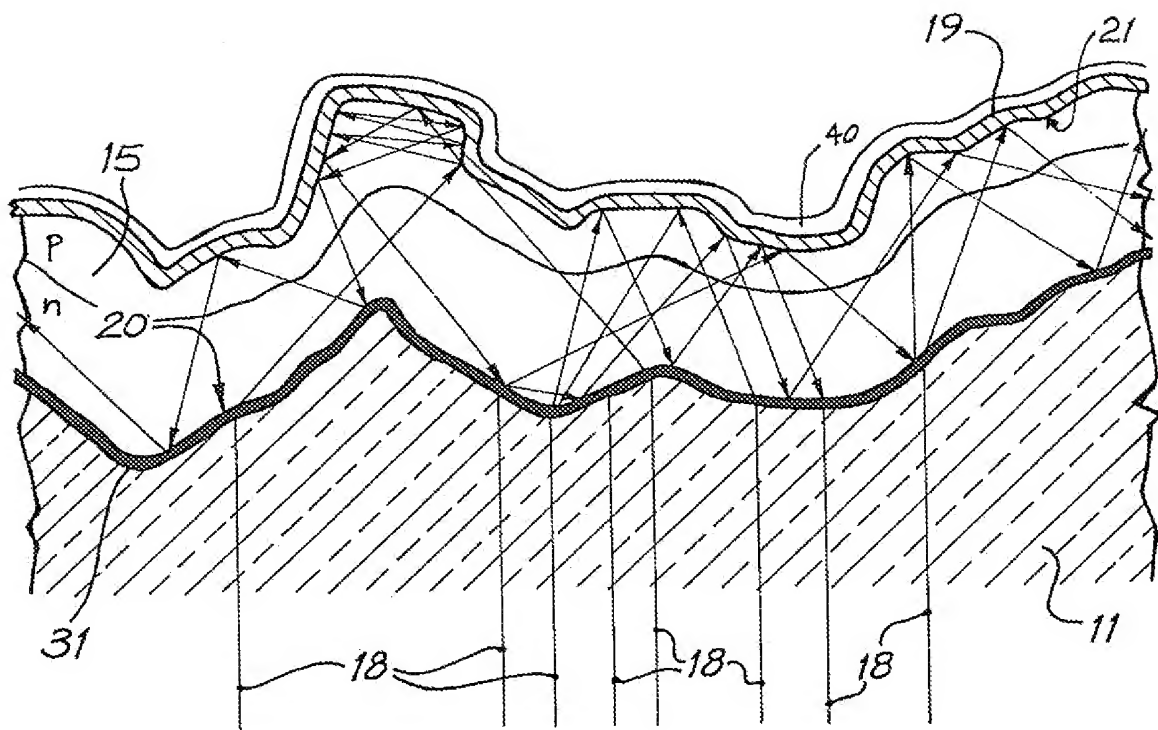


FIG. 5

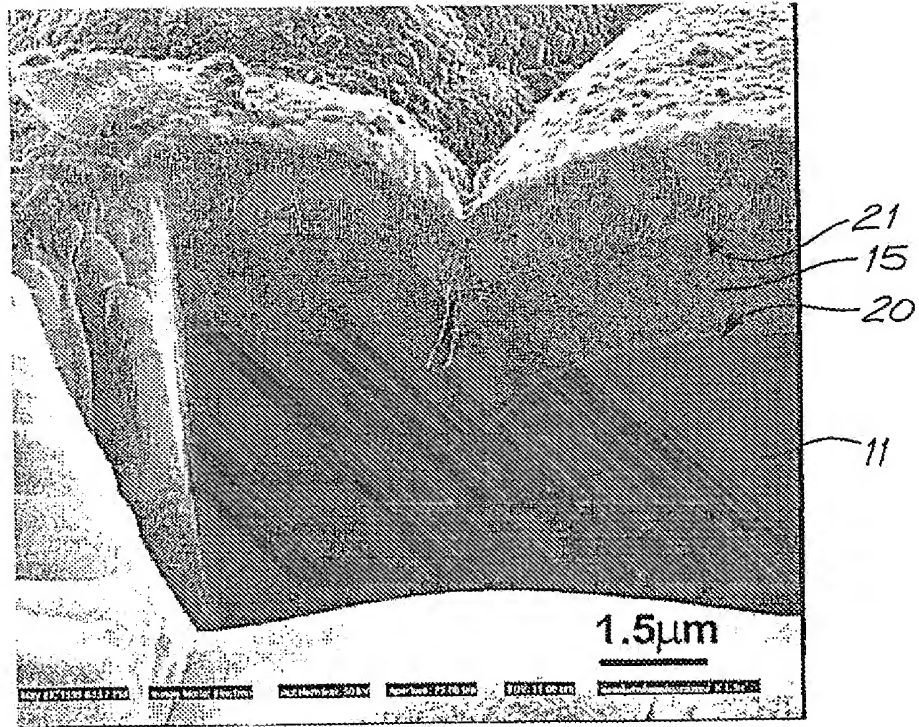


FIG. 6

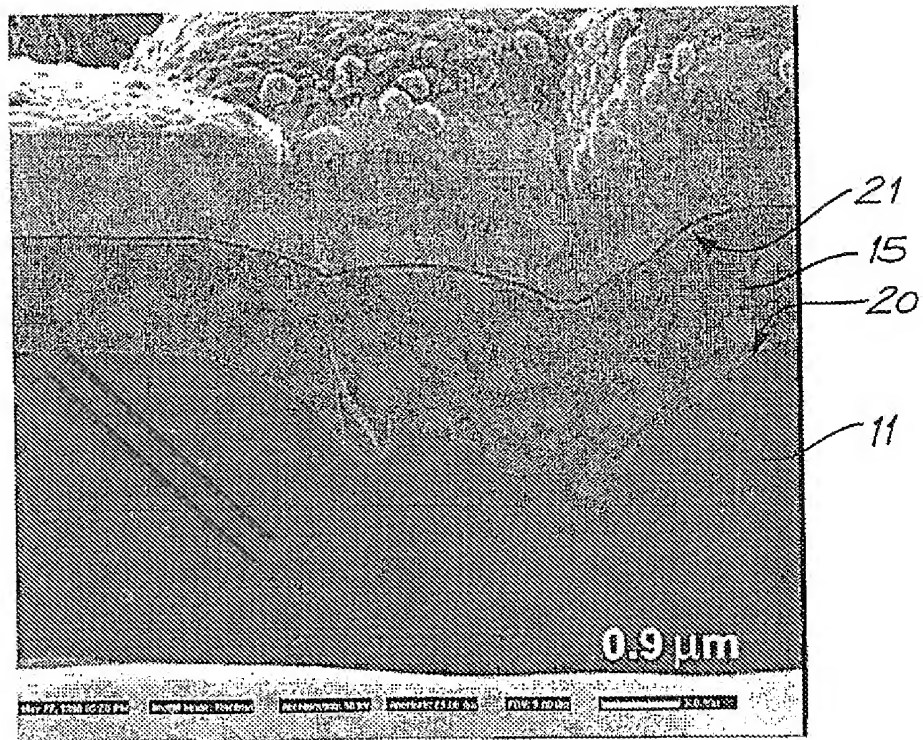
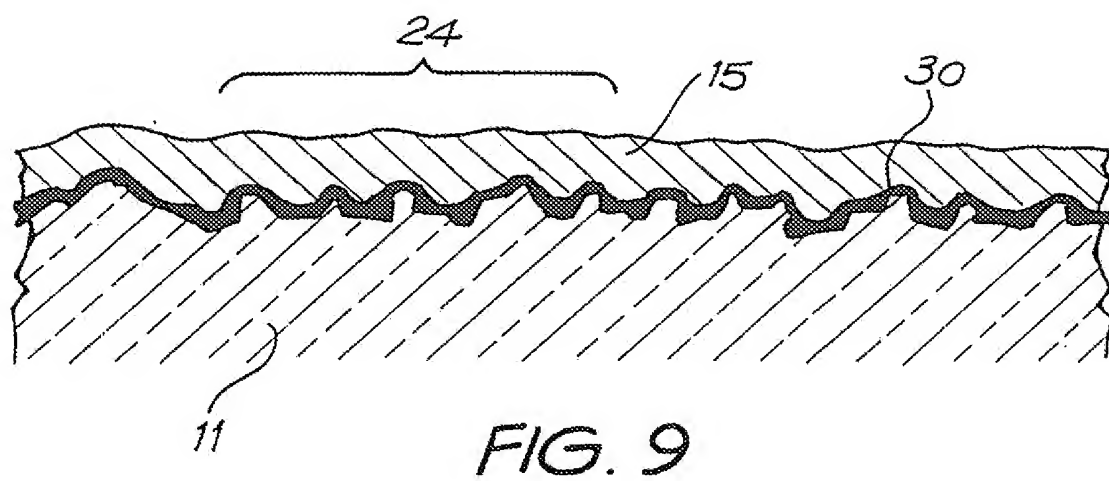
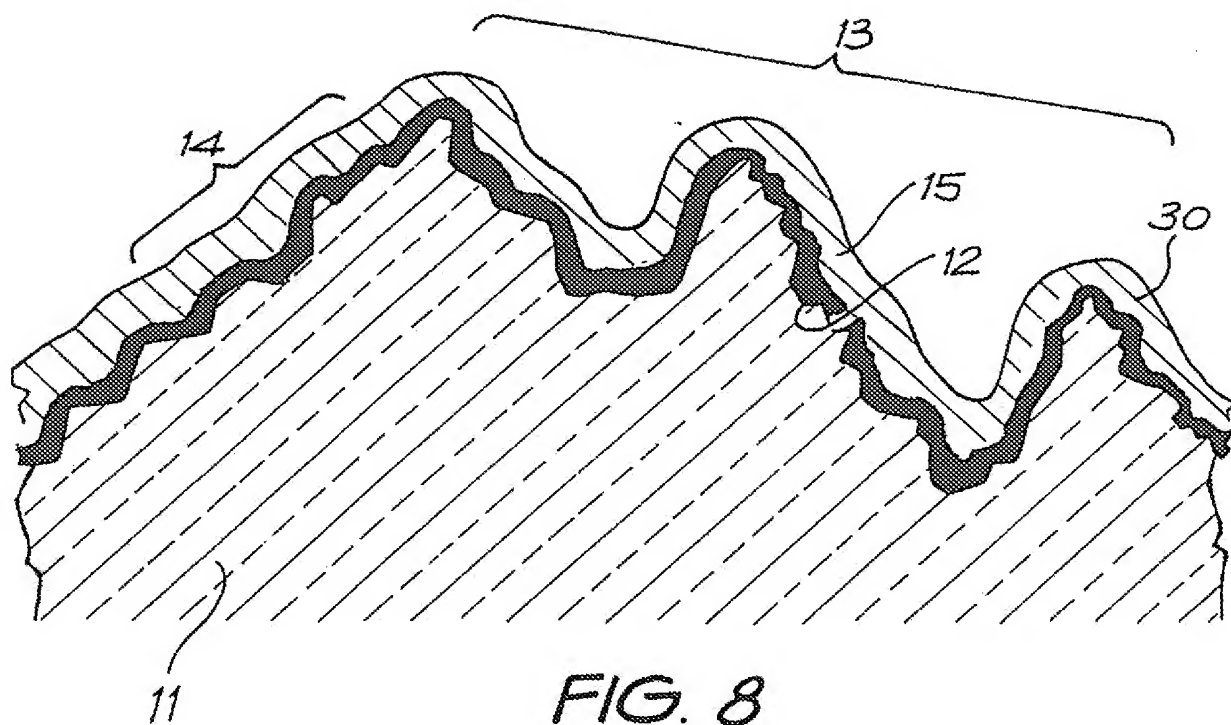


FIG. 7



INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU 99/80979

A. CLASSIFICATION OF SUBJECT MATTER																						
Int Cl ⁶ : H01L 31/0236 31/06 31/18																						
According to International Patent Classification (IPC) or to both national classification and IPC																						
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Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched AU : IPC as above																						
Electronic data base consulted during the international search (name of data base and, where practicable, search terms used) WPAT Keywords JAPIO																						
C. DOCUMENTS CONSIDERED TO BE RELEVANT																						
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.																				
X	US 4956685 A (FISCHER) 11 September 1990 See abstract and column 3 lines 29-36	1-44																				
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A	US 4732621 A (MURATA) 22 March 1988 See whole document																					
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<p>* Special categories of cited documents:</p> <table border="0"> <tr> <td>"A"</td> <td>Document defining the general state of the art which is not considered to be of particular relevance</td> <td>"T"</td> <td>later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention</td> </tr> <tr> <td>"E"</td> <td>earlier application or patent but published on or after the international filing date</td> <td>"X"</td> <td>document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone</td> </tr> <tr> <td>"L"</td> <td>document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)</td> <td>"Y"</td> <td>document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art</td> </tr> <tr> <td>"O"</td> <td>document referring to an oral disclosure, use, exhibition or other means</td> <td>"&"</td> <td>document member of the same patent family</td> </tr> <tr> <td>"P"</td> <td>document published prior to the international filing date but later than the priority date claimed</td> <td></td> <td></td> </tr> </table>			"A"	Document defining the general state of the art which is not considered to be of particular relevance	"T"	later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention	"E"	earlier application or patent but published on or after the international filing date	"X"	document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone	"L"	document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)	"Y"	document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art	"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family	"P"	document published prior to the international filing date but later than the priority date claimed		
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"O"	document referring to an oral disclosure, use, exhibition or other means	"&"	document member of the same patent family																			
"P"	document published prior to the international filing date but later than the priority date claimed																					
Date of the actual completion of the international search 07 January 2000		Date of mailing of the international search report 18 JAN 2000																				
Name and mailing address of the ISA/AU AUSTRALIAN PATENT OFFICE PO BOX 200 WODEN ACT 2606 AUSTRALIA E-mail address: pct@ipaustrialia.gov.au Facsimile No.: (02) 6285 3929		Authorized officer F.C. PEARSON Telephone No.: (02) 6283 2195																				

INTERNATIONAL SEARCH REPORT

International application No.
PCT/AU 99/00979

C (Continuation). DOCUMENTS CONSIDERED TO BE RELEVANT		
Category*	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0137291 A (KABUSHIKI KAISHA KOMATSU SEISAKUSHO) 17 April 1985 See abstract	
A	WO 88/09265 A (GLASSTECH SOLAR INC) 1 December 1988 See abstract	

INTERNATIONAL SEARCH REPORT
Information on patent family members

International application No.
PCT/AU 99/00979

This Annex lists the known "A" publication level patent family members relating to the patent documents cited in the above-mentioned international search report. The Australian Patent Office is in no way liable for these particulars which are merely given for the purpose of information.

Patent Document Cited in Search Report				Patent Family Member			
US	4956685	DE	3446807	FR	2578359	JP	61154183
		US	4931412				
US	4732621	JP	61288314	JP	61288473		
US	4719501	DE	3300400	JP	58118160	JP	58118161
		JP	58118162				
EP	137291	JP	60068663	US	4746372		
WO	8809265	EP	360831	JP	63313874	US	4808462
							END OF ANNEX